REMARKS

Claim 1-50 have been canceled.

New claims 51-81 have been added.

Claim 1, 4 and 7-10 were rejected on the ground of obviousness-type double patenting as being unpatentable over claims 1, 5 and 8-11 of U.S. Application 10/819086. This rejection is now moot.

Claims 1-16, 18-20, 23-28, 30-41 and 43-50 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tomasz in view of Keate, Birleson and MPEP 2144.04. This rejection is now moot.

New claim 51 recites an off-chip "surface acoustic wave filter" positioned between an unconversion stage and a zero-IF downconversion stage. The Examiner cites to Tomasz (US 6400416) which teaches a dual conversion receiver with an upconverter 222 and a downconverter 240 where the downconversion is of the zero-IF type. Positioned between the two converters in Tomasz is an off-chip filter 210. Tomasz teaches that this filter 210 is an LC filter (not a SAW filter). To meet the claimed SAW filter, the Examiner asserts that the use of a SAW, in place of an external LC filter between two conversion stages, is an obvious design choice. Applicants respectfully disagree.

There is no teaching or suggestion in Tomasz for the use of a SAW filter, and the Examiner has pointed to no prior art references which teach that an LC filter, in an implementation positioned to filter signals between an upconverter and a zero-IF downconverter, could be replaced by a SAW. Applicants assert that SAW filter technology would not be an

obvious design choice or substitution for an LC filter. The band pass characteristics of a SAW are different from that of an LC filter, and furthermore SAW filters are more complicated and more expensive to implement. Still further, the Examiner has not shown that one skilled in the art would choose a SAW implementation to filter a signal AFTER an RF upconversion frequency transposition. Additionally, there is no suggestion for implementing the SAW filter as an off-chip bandpass filter in the dual conversion frequency translator implementation claimed by Applicants.

New claim 51 further recites "a baseband filtering circuit that filters the baseband signal to generate a filtered analog baseband signal, the baseband filtering circuit having ***an upper cutoff frequency*** greater than a frequency half-width of one channel" and "an analog-to-digital converter circuit that converts the filtered analog baseband signal to a digital baseband signal, the analog-to-digital converter circuit having a ***sampling frequency which is at least ten times the upper cutoff frequency*** of the baseband filtering circuit". The prior art cited by the Examiner fails to teach the combination of the claimed baseband filter (with its upper cutoff frequency) and A-to-D converter (with its sampling frequency 10x the upper cutoff frequency). The Examiner has asserted that it is well known to sample at two times (2x) the signal bandwidth. However, there is no teaching in the cited art for, and it would not have been obvious to select, an at least ten times (10x) A-to-D sampling frequency.

New claim 51 still further recites "a digital baseband decimating filter." The prior art cited by the Examiner does not teach or suggest the use of a digital baseband decimating filter in combination with an at least 10x sampling A-to-D converter as claimed.

In view of the foregoing, Applicants submit that claim 51 and its dependent claims are in condition for favorable action and allowance.

New claim 63 recites "an analog low pass filter ... having an upper cutoff frequency", "an analog-to-digital converter ... having a sampling frequency which is at least ten times the upper cutoff frequency" and "a digital decimating low pass filter." These limitations are similar to those identified and discussed above with respect to claim 51, and claim 63 is asserted by Applicants to be patentable over the cited prior art for at the reasons recited above.

New claim 71 recites "analog low pass filtering ... having an upper cutoff frequency", "analog-to-digital converting ... having a sampling frequency which is at least ten times the upper cutoff frequency" and "digital decimating low pass filtering." These method limitations are analogous to the apparatus limitations of claim 63, and claim 71 is asserted by Applicants to be patentable over the cited prior art for at the reasons recited above.

New claim 73 recites "a baseband filtering stage ... having an upper cutoff frequency", "a multibit analog/digital conversion stage ... having a sampling frequency which is at least ten times the upper cutoff frequency" and "a digital decimation filtering stage." These limitations are similar to those identified and discussed above with respect to claims 51 and 63, and claim 73 is asserted by Applicants to be patentable over the cited prior art for at the reasons recited above.

New dependent claim 60 recites that "the single monolithic substrate further includes an oxide layer on a rear surface of the substrate" and that "a metal plate [is] glued to the oxide layer on the rear surface of the substrate to form a first plate of a capacitor, wherein a second plate of the capacitor is formed by the single monolithic substrate." The Examiner has asserted that it is

well known in the art to attach a metal plate to rear face of a substrate for the purpose of providing a heat sink. Applicants specifically claim that the metal plate, with an intervening oxide layer, forms a two-plate capacitor structure (the other plate being the substrate itself). The heat sink teachings mentioned by the Examiner do not suggest the formation of a capacitor structure as specifically claimed by the Applicants. See, also, claims 66 and 75.

New dependent claim 61 recites that "the metal plate is a grounded metal plate and the capacitor functions to absorb high-frequency current spikes." The heat sink teachings mentioned by the Examiner do not suggest the use of a capacitor structure with a grounded configuration to absorb (filter) high-frequency current spikes as specifically claimed by Applicants. See, also, claims 67 and 76.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

The Office is authorized to charge any additional claim fee necessary for entry of this response to deposit account 07-0153 (reference 361170-1028).

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